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Power Management by DVFS

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Abstract—The Power consumption in the most of the systems are important. Today most of the processors are working in GHz, so their Power consumption also goes on increasing. In this paper, we first review the basic mechanisms that underlie Power saving techniques. Then we survey two fundamental techniques for power saving. Based on these two techniques we can reduce power Consumption in significant level. This paper determines Minimum energy consumption in voltage and frequency Scaling systems for given time delay. Finally, we summaries and discuss future research directions.

Index Term –DVFS, linux, Arm, Power Management

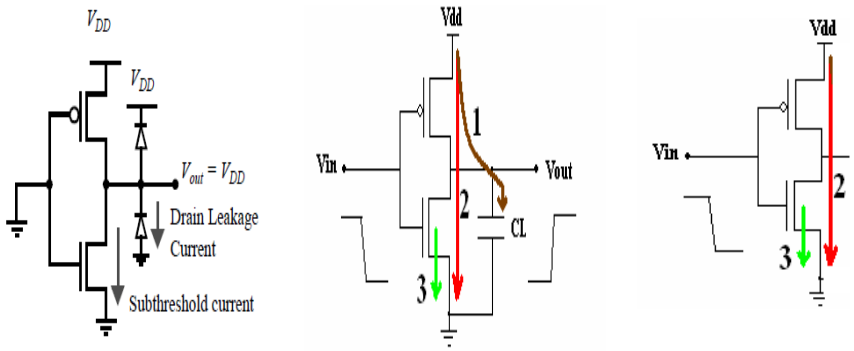
I. INTRODUCTION

Ongoing advances in CMOS process technologies and VLSI designs have resulted in the introduction of multicore processors. There is, however, the need to achieve high system –level performance without driving up the power dissipation. An important issue in hardware resource management is how to reduce power usage in processors. In the recent past, many hardware-based approaches have been made to efficiently reduce energy consumption, particularly for processors. Dynamic voltage-frequency scaling (DVFS) is perhaps the most appealing method incorporated into many recent processors. Energy savings with this method is based on the fact that the power consumption in CMOS circuits has direct relation with frequency and the square of voltage supply. In this case, the execution time and power consumption can be controlled by switching between processor's frequencies and voltages [1].

Today most of the processors mainly develop from cmos technology, especially processors, therefore the analysis of power dissipation in CMOS circuits is essential to find out the relation between power, supply voltage, and clock frequency. The power dissipation for CMOS circuits is the summation of dynamic power, static power and short circuit power. These components of power dissipation is as shown in Figure 1 are because of **[2],**

1. Pdynamic which is due to charging and discharging capacitors.
2. Pstatic which is due to reverse biased diodes.
3. Pshortcircuit which is due to switching direct path between Vdd-GND.

The different power dissipations are figurout as shown below-



The dynamic power is the main portion of the CMOS power dissipation [2]. It can be expressed as:

Pdynmaic CL Vdd 2 fclk.
Where CL is the collective switching capacitance, Vdd is the supply voltage, and fclk is the clock frequency. The high power dissipation of a processor has at least the following disadvantages:

- High power systems tend to run hot, that causes the processor and other system components to fail. The failure rate of a processor is doublesevery 10oC increase [2].
- It complicates the cooling solutions of integrated circuits for heat removal, and thus increase the production cost. Intel estimates that more than 1$/W per processor chip will be added once the processor power dissipation exceeds 35-40 W [3].
- It increases the operation costs; such as the electricity bills for air conditioning of the computer and system rooms. 8% of US electricity in 1998 was attributed to the internet, growing to about 30% by 2020 [4].
- It shortens the battery or UPS life. The processor power doubles every four years, consequently the average battery or UPS life will be shortened [5].

II. EXPERIMENTAL FRAMEWORKS

Technology Parameters and DVFS Settings: We use process parameters for a 70nm CMOS technology and we assume that the highest supply voltage (*Vmax*) is 1V and the highest clock frequency (*fmax*) is 4 GHz. During frequency scaling, the vo tage is scaled according to the equation. As we show later in this paper, our methodology does not depend on the exact relationship between *V-f* (this relationship is simply an input to our models). F nally, we assume that the processor's effective capacity (*Cload*) remains constant across different *V/f* settings [6].
Static Power Consumption: In this work, we consider only dynamic power/energy as our target for optimization. However, our methodology can be easily extended to include leakage power; typically known during manufacturing for a range of *V,f* settings [6].
On-chip and Off-chip Voltage Regulators: Traditionally, the full promise of the DVFS has been hindered by slow off-chip voltage regulators. The time overhead to switch the supply voltage using off-chip voltage regulators is in the order of microseconds and is also accompanied by a significant energy overhead [7]. Recently, significant work has been performed on integrating voltage regulators on-chip. On-chip voltage regulators offer fast voltage transitions at nanosecond time-scales and are much smaller in size compared to the off-chip voltage regulators. Unfortunately, their benefits are hampered by lower energy-conversion efficiencies. Thus, there is a trade-off between the size of the voltage regulators, the transition time they offer, and their conversion efficiencies. This trade-off is explored by Kim et. Al. [7], in the context of a CMP system where per-core DVFS (using on-chip regulators) as well as chip-level DVFS (using off-chip regulators) were utilized. Our methodology does not depend on the time-scale in which DVFS decisions are taken. The two analytical models presented in the next section are able to drive informed DVFS decisions by exploring the slack due to long-latency, off-chip, memory operations, but over user-selected portions of the program [6].

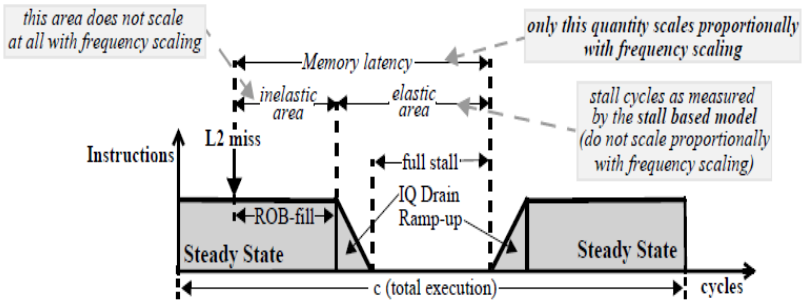


Fig. 1 Useful instructions issued per cycle in the case of an isolated L2 load miss.

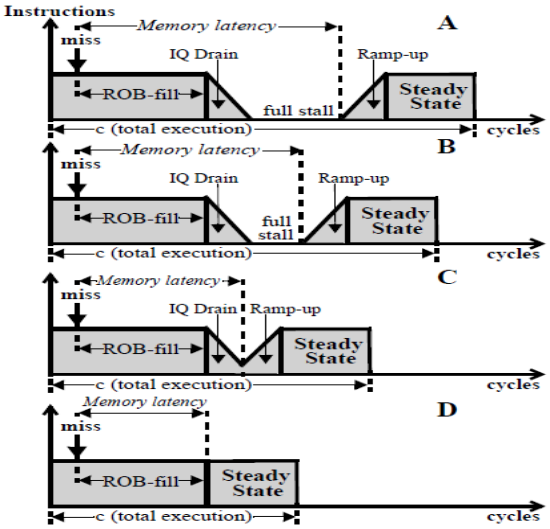


Fig 2. Useful instructions issued per cycle: case studies under different frequencies.

III. Equations

Reducing the supply volatgge also reduce the system power due to the relation between the power and vdd is-

On the basis of relations in dynamic power, voltage & frequency,

$P_{dynmaic} \alpha CL\ Vdd^2\ f_{clk}$ ….fig (a)

$P_{dynmaic} \alpha V\ f_{clk}/2$ …fig (b)

$P_{dynmaic} \alpha V/2\ f_{clk}$ … fig (c)

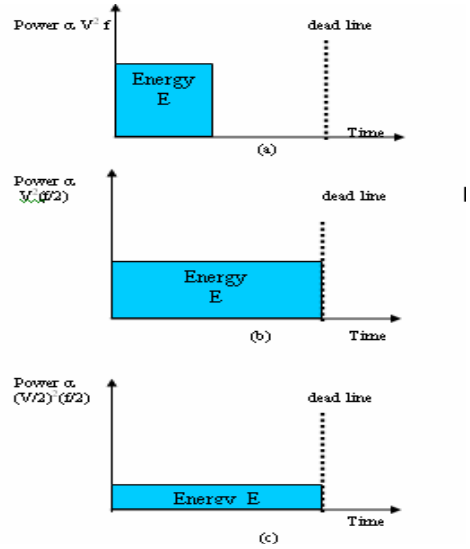


Fig:-3 Energy consumption vs. power consumption With DVFS

IV. IMPLEMENTATION

- Tree main tools of DVFS power management:
  1. Operating System: It provides different speed requiments to the processor to perform different muti-speed functions of processor.
  2. Control Loop: It generates different voltage levels to processor to accomplish the different functions with desired speed requirement.
  3. Processor: It's operates on different range of volteges.

- The following figure shows how these three controlling actions are co-ordinates with each other-

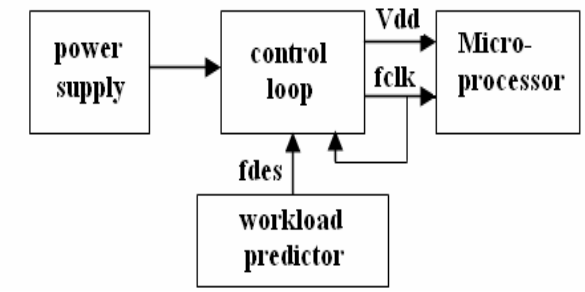


Fig 4 controling action

- Workload predictor plays main role in the operation of DVFS.

Workload Predictor:

The modern operating system will intelligently vary the processor speed to perform the muli-speed functionality of processors by predict and estimate the future workload of the processor and convert it to a digital word (fdes) and save it into a register, whose value is then used by the control loop to adjust the processor clock frequency (fclk) with the voltage level (Vdd) **[**8**].**

The workload of the processors usually consists of sequence of tasks and idles between tasks.The processors goes to sleep as a result of some special instruction and wake up by some interrupt this cause producing idle intervals between the task.By using DVFS tech we can extend each task till ideal time and we can reduce system workload.

The concept of an event makes partitioning the workload to be possible. Two parameters, □□and □□as shown in figure, are used to describe an event; both in the unit of time, □□measures the length of an event and □ measure the length of an event plus idle time before the next event starts.

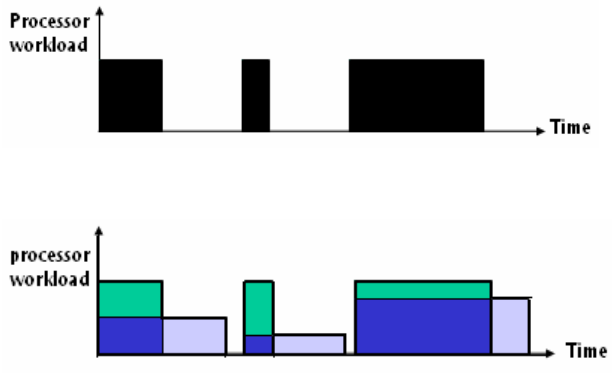


Fig 5- A typical workload pattern with tasks and idle time between tasks.

It follows that utilization can be determined by dividing □□by □ for example if utilization is 50 percent, it means that this particular event has the potential to be scaled down by a factor of two [8, 9].

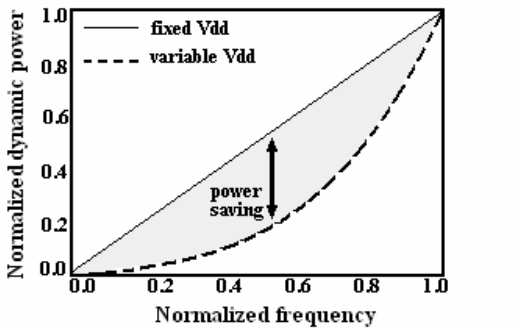


Fig:6- with dvfs we can save power that has been denoted by shaded portion

Thus as shown in the adove figure,as the frequency goes on increasing power consum by the system goes high, by using DVFS tech if,frequency is reduce then power consum by the system also get reduce.

V. TOOLS

- **Linux-** Windows 7 by default has very minimal software set, the basic features that we need – word processor, spread sheet and presentation software are not present. You'll have to purchase and install the MS Office suite separately; this is something that should be bundled with the operating system. On the other hand Ubuntu 12.04 comes with the LibreOffice suite (a Microsoft Office Equivalent) preinstalled. It also has F-spot, an image editing program that and an Instant messaging client called Empathy – that has chat provisioning for Facebook, G-Talk, Yahoo,MSN and VOIP capabilities all under a single application.

  Drivers – One of the biggest advantages of Linux is its built-in driver set, or rather the ability of automatically downloading and installing them. This includes the drivers for your webcam, Wi-Fi, Ethernet Card, even your printer or scanner! We all know drivers are a big pain that comes when completing a fresh install of Windows 7. With Linux, there is rarely any need to download the drivers manually. Linux also has the ability to download proprietary drivers (The ones from Nvidia and ATI), unlike windows where we have to manually download and install a driver for everything [11].

Why Ubuntu 12.04-

Unity Improvements-"If you don't want to see a specific content source it will remember it. If you don't want to see applications that are available for download, you just deselect the software centre from the list."

You can now turn off sources for the Dash, for example you can remove results from the software centre while searching for a specific program.
With the popularity of programs such as MyUnity, allowing you direct control over some of the more advanced Unity settings in a graphical interface, Canonical have decided that now is the time to give users an "official" way to tweak the environment-BY Neil Patel [12, 13].

HUD-HUD learns from your actions, deploying a weighting system for menu options based on your usage history. Patel specifically said that there's a 30 day expiration period for menu options you've only used once, resetting their weighting. There are no HUD "profiles" as such, so your settings and preferred search terms won't sync over, say, Ubuntu One between machines.

ARM- Ubuntu for Android is made possible from the increased ARM support with the recent

announcement of Ubuntu for Android and its subsequent demos at Mobile World Congress, getting the full Ubuntu OS running on ARM has been a priority. Dave Walker, Technical Lead for Ubuntu Server, gave us some insight on its development over the past 6 months

"It's because of the amount of computing power you can get into a small area, the significantly lower power consumption, and because of all that it's much cooler [12, 13].

Server Upgrades-Ubuntu Server is extremely popular among enterprise users and administrators, with a recent survey finding that is was one of the most pervasive server operating systems. As an LTS release, the new server edition is going to be desirable for a lot of sysadmins [12, 13].

Stability-Due to its LTS promise, the development cycle has focused more on improving the core experience and fixing bugs, as well as a fit-and-finish approach to UI elements.Unity's Dash has been upgraded to give users more control [12, 13].

- **OMAP3430-**

1. The first device in TI's OMAP™ 3 architecture, the OMAP3430 multimedia applications processor delivers up to 3x gain in performance over ARM11-based processors, enabling laptop-like productivity and advanced entertainment in mobile devices. The industry's first application processor to be designed in a 65-nanometer (nm) CMOS process, the OMAP3430 operates at a higher frequency than previous generation OMAP processors while lowering the core voltage and adding power reduction features.
2. ARM® Cortex™-A8 superscalar microprocessor core. Combined with TI's technology in the OMAP3430,
3. With TI's DaVinci™ technology that provided 4x performance improvement in multi-media processing.
4. The OMAP3430 processor embeds Imagination Technologies' POWERVR SGX™ graphics core, and supports OpenGL ES® 2.0 and OpenVG™, providing superior graphics performance and advanced user interface capabilities.
5. The OMAP3430 can connect to images sensors up to 12 megapixels in size with minimal shot-to-shot delay [10].

VI. CONCLUSION

We have analyzsed that DVFS technique that we are going to implement with OMAP 3430 which can be save power, acting as a voltage regulator. The DVFS technique can decreases the processors average energy consumption at runtime depending on the applications and the limit of the supply voltage Vdd. When transition time is short (compared to task periods), Power saving is larger.

VII. ACKNOWLEDGMENT

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